WE CLAIM:

1. An integrated memory, comprising:

a memory cell array, the memory cell array having word lines for the selection of memory cells and bit lines for reading out or writing data signals of the memory cells, the bit lines being organized in bit line pairs, the bit lines of one of the bit line pair crossing one another at a crossing location and running parallel to one another;

a sense amplifier, which is connected to one of the bit line pairs at one end of the bit line pair;

two precharge circuits, the precharge circuits being connected to one of the bit line pairs in order to precharge the bit lines of the bit line pair to a precharge voltage, one of the precharge circuits being arranged on a side of the crossing location which faces the sense amplifier, the other of the precharge circuits being arranged on a side of the crossing location which is remote from the sense amplifier,

the first precharge circuit facing the sense amplifier being arranged at a first distance from the crossing location and at a second distance from the sense amplifier, the first distance being less than the second distance.

2. The integrated memory as claimed in claim 1, wherein at least one of the precharge circuits is arranged within a region, the region being relatively smaller in relation to the memory cell array and being arranged centrally in relation to the longitudinal extent of the relevant bit line pair.

3. The integrated memory as claimed in claim 1, wherein at least one of the precharge circuits has a precharge transistor, the controlled path of the precharge transistor being connected to a terminal for a supply voltage of the memory and to one of the bit lines of the respective bit line pair.

4. The integrated memory as claimed in claim 1, wherein at least one of the precharge circuits has a switch, the bit lines associated with the respective bit line pair being connected to one another via the switch.

5. A method for operating an integrated memory, the integrated memory including a memory cell array, the memory cell array having word lines for the selection of memory cells and bit lines for reading out or writing data signals of the memory cells, the bit lines being organized in bit line pairs, the bit lines of one of the bit line pair crossing one another at a crossing location and running parallel to one another;

a sense amplifier, which is connected to one of the bit line pairs at one end of the bit line pair;

two precharge circuits, the precharge circuits being connected to one of the bit line pairs in order to precharge the bit lines of the bit line pair to a precharge voltage, one of the precharge circuits being arranged on a side of the crossing location which faces the sense amplifier, the other of the precharge circuits being arranged on a side of the crossing location which is remote from the sense amplifier, the first precharge circuit facing the sense amplifier being arranged at a

first distance from the crossing location and at a second distance from the sense amplifier, the first distance being less than the second distance, comprising:

activating one of the word lines at the beginning of a memory access to select one of the memory cells;

passing the charge stored in one of the memory cells to one of the bit lines;

passing the charge from the last line to the sense amplifier, which spreads the respective bit lines;

writing back the signal stored in one of the memory cells to one of the memory cells again; and

activating a control line for driving one of the precharge circuits, after the deactivation of one of the word lines, so that the bit lines of a bit line pair are short-circuited and precharged.

6. The integrated memory as claimed in claim 5, wherein at least one of the precharge circuits is arranged within a region, the region being relatively smaller in relation to the memory cell array and being arranged centrally in relation to the longitudinal extent of the relevant bit line pair.

7. The integrated memory as claimed in claim 5, wherein at least one of the precharge circuits has a precharge transistor, the controlled path of the precharge transistor being connected to a terminal for a supply voltage of the memory and to one of the bit lines of the respective bit line pair.

8. The integrated memory as claimed in claim 5,

wherein at least one of the precharge circuits has a switch, the bit lines associated with the respective bit line pair being connected to one another via the switch.